High-performance InGaAs/InP-based single photon avalanche diode with reduced afterpulsing

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ABSTRACT

We report reduced afterpulsing for a high-performance InGaAs/InP single photon avalanche photodiode (SPAD) using a gated-mode passive quenching with active reset (gated-PQAR) circuit. Photon detection efficiency (PDE) and dark count probability (DCP) were measured at a gate repetition rate of 1 MHz. With a double-pulse measurement technique, the afterpulsing probability was measured for various hold-off times. At 230K, 0.3% afterpulsing probability for a 10 ns hold-off time was achieved with 13% PDE, 2×10^{-6} DCP and 0.4 ns effective gate width. For the same hold off time, 30% PDE and 1×10^{-5} DCP was achieved with 6% afterpulsing probability for an effective gate width of 0.7 ns.

Keywords: afterpulsing, dark count probability, passive quenching with active reset, photon detection efficiency, and single photon avalanche diodes.

1. INTRODUCTION

High performance single photon detectors have emerged as viable components for many applications, such as quantum communication,[1] biological imaging,[2] circuit testing,[3] and laser ranging.[4] InGaAs/InP single photon avalanche diodes (SPADs) achieved high photon detection efficiency (PDE) and low dark count rate (DCR) in the near-infrared (NIR) wavelength range between 1.0 and 1.7 μm.[5,6]

However, for many applications afterpulsing is a significant performance limitation for infrared SPADs. The ultimate solution to eliminate or reduce afterpulsing is to improve the material quality and reduce the deep level traps. With current materials technology, however, alternative approaches must be developed. One effective approach is to reduce the charge flow through the device during an avalanche breakdown, Q_A, in order to reduce the number of trapped carriers. In gated quenching, since the diode is both armed and quenched by the applied gate pulses, Q_A increases with wider pulse widths. Using very narrow pulse widths, ~100 ps, has been shown to be a viable technique to reduce Q_A.[7,8,9] However, it generally requires very high gate pulse height (>10V V_{p-p}) in order to reduce the avalanche build-up time and achieve useful PDE (>10%). More importantly, very complicated techniques are required to detect the faint avalanche signal submerged in the large background noise. Passive quenching provides another method to reduce Q_A. In passive quenching, Q_A can be limited to the product of the excess bias, V_{ex}, and the total capacitance, C_{total} (including the diode capacitance, C_{diode}, and the stray capacitance, C_{stray}).[10] Active quenching circuits (AQCs)[11] on the other hand have the advantages of better defined hold-off time and more uniform PDE, thanks to their fast recharge of the device bias compared to passive quenching. However, when C_{total} is less than 1 pF, the quenching time for passive quenching is generally comparable to or even shorter than the feedback time of the active quenching circuit (a few nanoseconds), in which case, active quenching is not necessary for the quenching function. In order to take the advantage of the benefits of both the simplicity of passive quenching and the fast recharge of active quenching, we have developed a passive quenching with active reset (PQAR) circuit for operation in the free-running mode.[12,10,13] The idea of PQAR has also been extended into gated mode operation, which we will refer to as gated-PQAR.[14]

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In this paper, we report a high-performance InGaAs/InP SPAD with an improved gated-PQAR circuit. The stray capacitance C_{stray} has been reduced, compared to an earlier report on gated PQAR,[14] by chip-to-chip wire bonding, which has contributed to a significant reduction in afterpulsing.

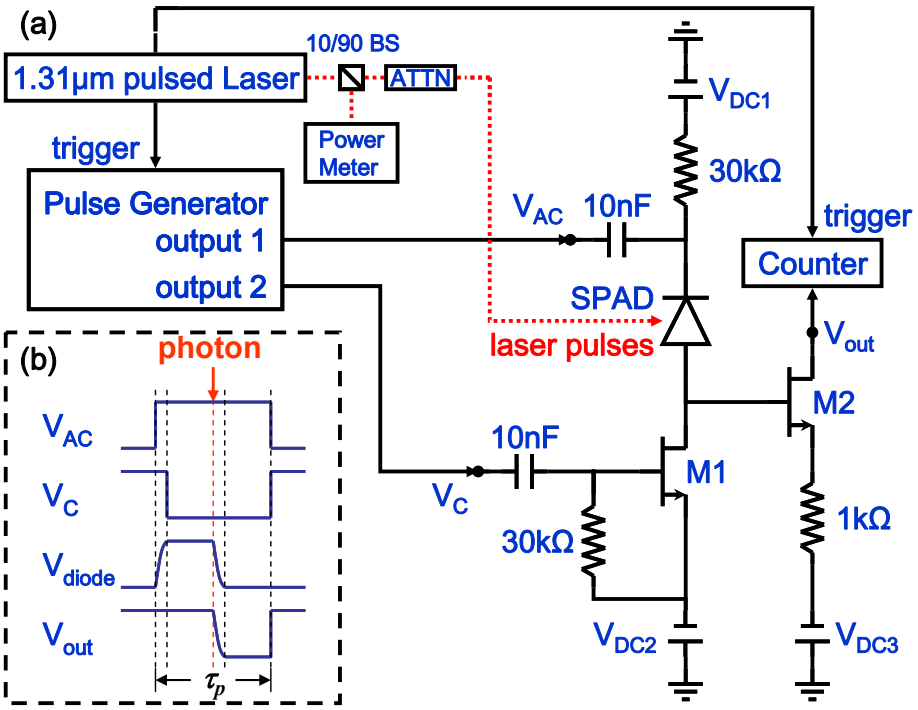

Figure 1. (a) Equivalent circuit for the improved gated-PQAR circuit and (b) its operation mechanism.

2. EXPERIMENT AND DISCUSSIONS

Figure 1(a) shows the equivalent circuit of the improved gated-PQAR circuit. The basic operation mechanism of the gated-PQAR circuit is very similar to that of the conventional gated quenching circuits. The SPAD is biased at a DC voltage, V_{DC1}, below the breakdown voltage, V_{br}, through a 30 kΩ load resistor. As shown in Figure 1(b), the diode is periodically biased with an excess bias, V_{ex}, above the breakdown voltage by gate pulses, V_{AC}, coupled through a 10 nF capacitor; this defines the detection windows. After a small delay that is sufficient to fully charge the diode up to the detection bias, a control pulse, V_C, is sent to turn off the quenching transistor, M1. The high off-state impedance of M1 insures that, once an avalanche is triggered, the avalanche current will quickly discharge the diode and reduce its bias, V_{diode}, therefore, which will terminate the avalanche event. The decrease of V_{diode} results in an increase of the anode bias, V_A, which is picked up by the sensing transistor, M2. The negative transition of the M2 output voltage, V_{out}, marks the arrival time of the photon, and will be registered at the counter. At the tailing edge of V_{AC}, M1 will be turned back on by V_C. Therefore, regardless of whether an avalanche is triggered, everything will be reset until the next detection window.

We note that the addition of M2 in the improved gated-PQAR circuit eliminates the difficulty of discriminating between true avalanche events and the spurious detection of transients related to the fast recharge of the SPAD. Unlike the previous PQAR circuits, in which the counter senses the avalanche current pulse with fixed input impedance, M2 serves as an amplifier with variable input impedance determined by M1. During recharging, M1 is turned on. Owing to its low on-state impedance, M2 will not pass the recharge transient to the counter. On the other hand, when M1 is turned off, M2 will have extremely high input impedance to easily sense the onset of an avalanche.

In the improved gated-PQAR circuit, instead of using discrete components, the SPAD and the two GaAs FETs are unpackaged chips directly mounted on a sapphire carrier, where low-parasitic chip-to-chip wire bonding was employed to minimize the stray capacitance C_{stray} associated with the anode of the diode. Since it is difficult to monitor the

avalanche-current output of the gated-PQAR, in order to investigate the reduction of Q_A, we have compared the avalanche-current-pulse outputs of two of our PQAR circuits, one built with discrete components and one built with chip-to-chip wire bonding. As shown in Figure 2, the one with chip-to-chip wire bonding shows approximately a factor of 16 of reduction in Q_A. The reduction of Q_A results in more than an order of magnitude lower afterpulsing probability (Figure 3).

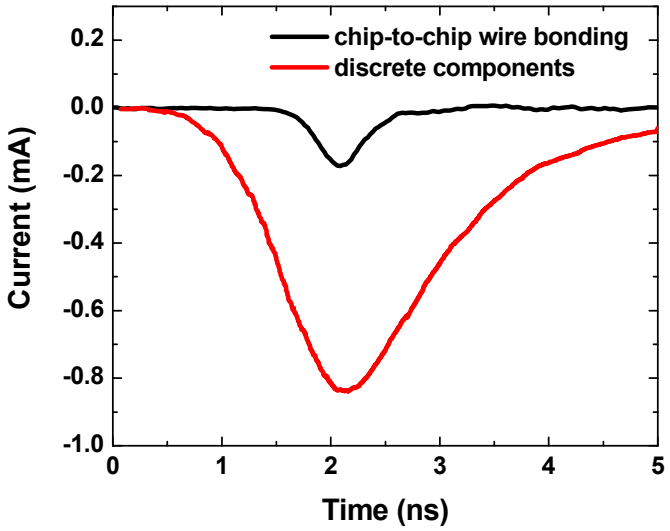

Figure 2. Avalanche-current-pulse outputs of two PQAR circuits under similar excess bias.

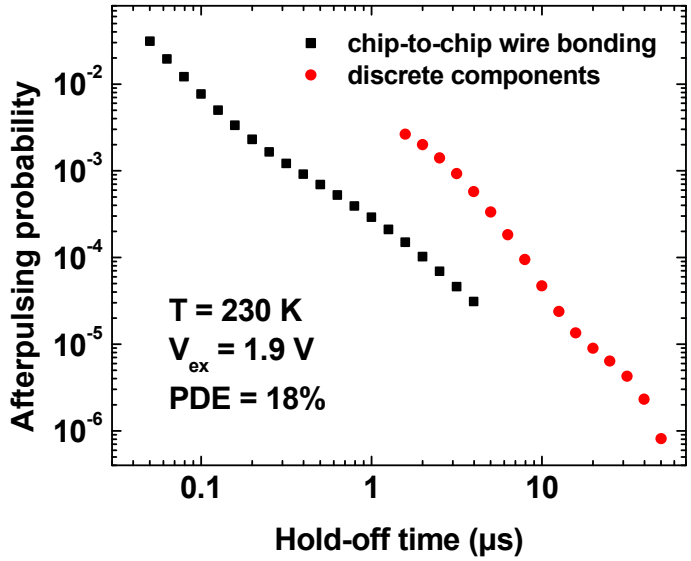

Figure 3. Equivalent afterpulsing probability per ns gate versus hold-off time for comparison of PQAR circuits built with two techniques.

The SPAD under test is a 25-μm-diameter planar InGaAs/InP-based SACM APD grown by metal-organic chemical vapor deposition (MOCVD).[15] With the improved gated-PQAR circuit, we were able to obtain extensive data on this

SPAD for dark count probability (DCP), photon detection efficiency, and afterpulsing probability (APP) for gated mode operation at a repetition rate of 1 MHz (limited by the pulsed laser driver). Figure 4 shows the measured DCP versus PDE under different excess biases and pulse widths at 230K. For the same excess bias, when the pulse width is shorter than a certain value, both the DCP and PDE drop much faster, which indicates that the effective gate width is shorter than the nominal pulse width set in the pulse generator. Also, the difference between them is larger at lower bias, due to the longer avalanche build-up time. Figure 5 shows the linear fit between the DCP and the pulse width. In intrinsic DCR can be extracted from the slope of the linear fit, and the x-intercept indicates the difference between the pulse width and the effective gate width. In this case, the 3.5 V excess bias gives a DCR of 16 kHz and the 2 ns pulse has an effective gate width of 0.7 ns. Similar measurement and calculation were applied for different temperatures (Figure 6).

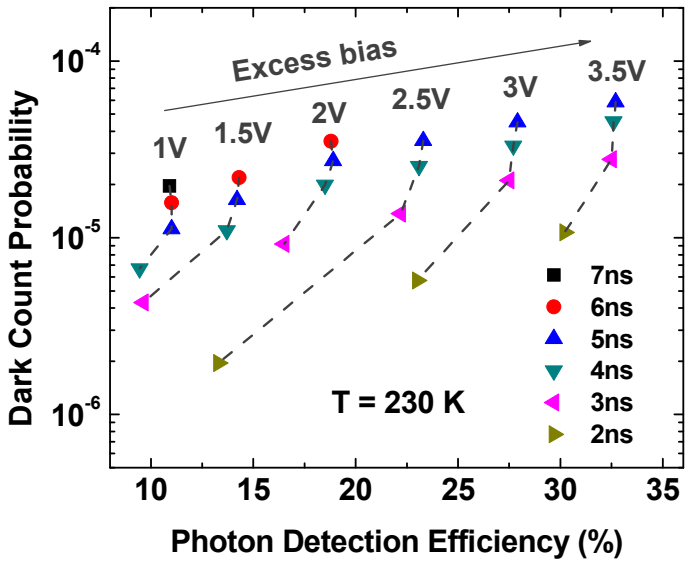

Figure 4. Dark count probability vs. photon detection efficiency at 230K. The different symbols denote the pulse widths set in the pulse generator.

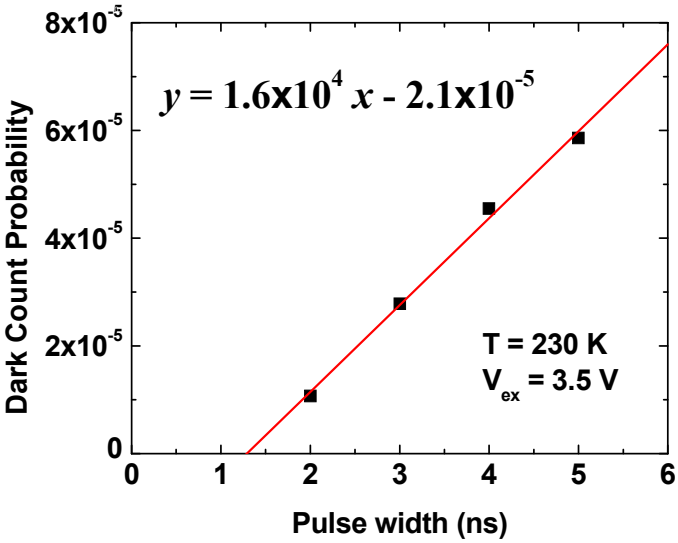

Figure 5. Dark count probability vs. pulse width at 230K with 3.5 V excess bias.

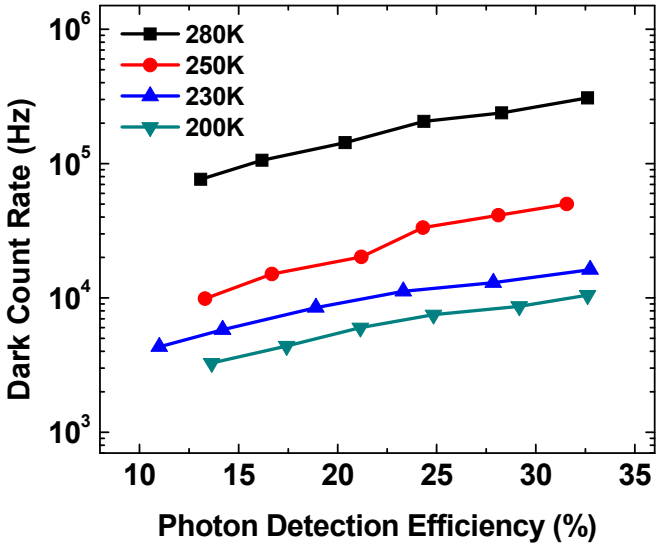

Figure 6. Dark count rate vs. photon detection efficiency for gated-mode operation at 1 MHz repetition rate with the improved gated-PQAR circuit.

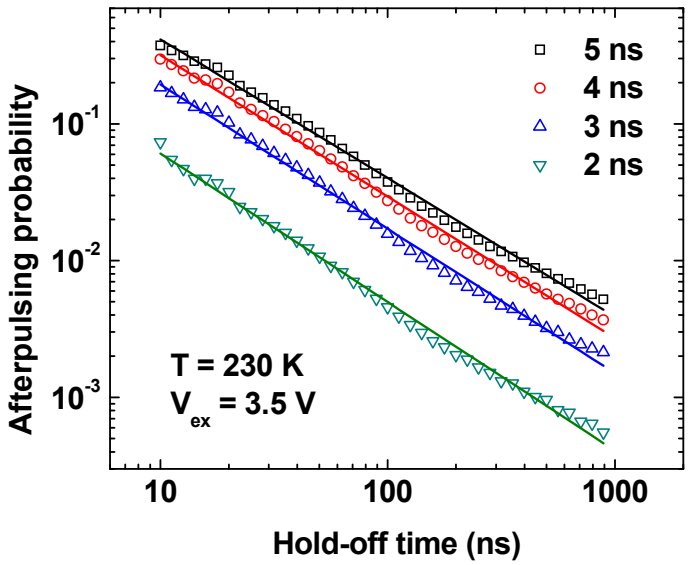

Figure 7. Afterpulsing probability vs. hold-off time for different pulse widths at 230K with 3.5 V excess bias. Solid lines are the linear fits of data in log-log scale.

The characterizing of afterpulsing was implemented by the double-pulse method.[16] In this technique, two gate pulses are used with a variable delay (hold-off time) between them. During the first gate pulse, the detector is illuminated with a sufficiently large optical pulse to guarantee that an avalanche occurs. When the second gate pulse is applied to the detector after a specified hold-off time, the detection of an avalanche signals the occurrence of an afterpulse. The contribution of non-afterpulse dark counts can be subtracted by the dark count probability measured. As shown in Figure

7, the afterpulse probability decreases roughly as the inverse of the hold-off time: the solid lines are apparent linear fits with a slope of approximately −1 on a log-log plot. Similar trend is observed for all the operation conditions.

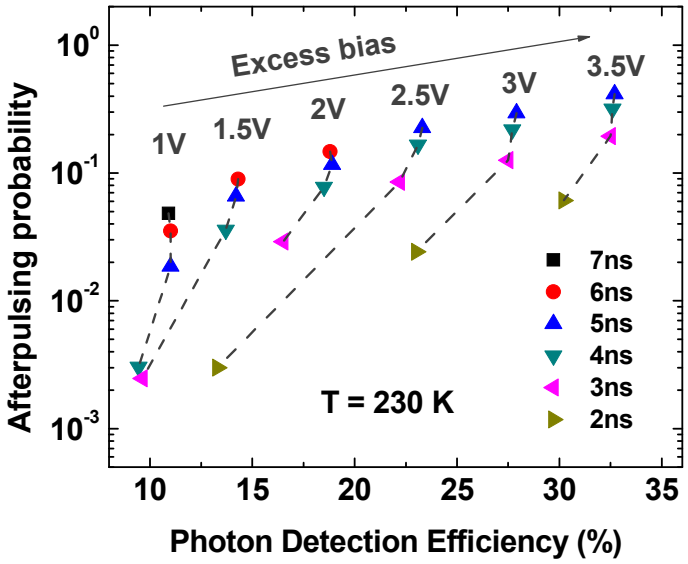

Figure 8. Afterpulsing probability vs. photon detection efficiency at 230K for 10 ns hold-off time between the two pulses. The different symbols denote the pulse widths set in the pulse generator.

The afterpulsing probability also varies with the pulse width (Figure 8) in a similar way to the dark count probability as in Figure 4. From both of the figures we can see that, for the same PDE, a combination of higher excess bias and shorter pulse width always gives better dark count and afterpulsing performance. For a PDE of 30%, 1×10^{-5} dark count probability and 6% afterpulsing probability for 10 ns hold-off time was achieved with 3.5 V excess bias and 2 ns pulse width. For a lower PDE of 13%, 2×10^{-6} dark count probability and 0.3% afterpulsing probability for the same hold-off time was achieved by reducing the excess bias to 2.5 V. At 2.5 V excess bias, although the PDE with 2 ns pulse width drops for almost half of the PDE with longer pulse width, there is still 0.4 ns of the effective gate width (FMHW, measured by scanning the relative laser position within the gate pulse). As long as the effective gate width is tolerable, better trade-off can be achieved with even narrower pulse width.

3. CONCLUSION

In summary, we reported a high-performance InGaAs/InP SPAD tested in an improved gated-PQAR circuit with a significant reduction of afterpulsing thanks to the low-parasitic chip-to-chip wire bonding between the diode and the two FETs. At 230K, 0.3% afterpulsing probability for a 10 ns hold-off time was achieved with 13% PDE and 2×10^{-6} dark count probability. For the same hold off time, 30% PDE and 1×10^{-5} dark count probability was achieved with 6% afterpulsing probability.

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